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ABSTRACT

A method is described for accurately predicting nonlinear microwave performance of GaAs MESFET devices. The method utilizes time-domain analysis and is based upon experimentally characterized bias-dependence of device circuit model elements. Precise predictions are made of fundamental and harmonic power levels up to 6 dB of gain compression.

Introduction

An accurate nonlinear device model is a valuable tool for establishing microwave performance limits of GaAs FET devices. Model predictions of gain-compression, harmonic and intermodulation distortion will assist in the design of large-signal components such as power amplifiers, oscillators and harmonic generators. Linear models which describe small-signal electrical performance of GaAs FET's have been reported in the literature. Analytical expressions for calculating the bias dependence of some of the linear model element values have also been developed. However, no accurate large-signal GaAs FET model has been established.

The investigations outlined below focus on the derivation of a comprehensive nonlinear circuit-type device model. It evolves from the experimentally determined bias and frequency dependence of the device scattering parameters. The model was used in a time domain analysis program to simulate large signal waveforms. The simulations were made with the device in a common source configuration and mounted in a 50 ohm system. The output waveforms were transformed into the frequency domain by Fourier analysis. The excellent agreement obtained between experiment and model predicted gain compression, third-order intermodulation and harmonic output power levels demonstrate the model validity.

Device Characterization

The work described in this paper is based upon an arbitrarily selected Texas Instruments, Inc. GaAs MESFET. This device has the following parameters:

Gate Width, l_w	= 600 μ m
Gate Length, l_g	= 1.7 μ m
Doping Density, N_D	= 7.5×10^{16} cm $^{-3}$
Epitaxial Thickness, a	= 0.3 μ m

The measured $I_{DS}V_{DS}$ curves are illustrated in Figure 1. The modeling of the nonlinear device behavior was predicated on experimentally determined bias-dependence of its small signal characteristics. The topology of the circuit-type model is identical to that of the linear model [1] previously developed to include Gunn domain effects (See Figure 2). The bias-dependence of each element of the linear model was determined by least-square fitting of model predicted small-signal S-parameters to measured S-parameters for various bias conditions. The measurements were taken across the frequency range of 1-10 GHz for discrete combinations of drain-to-source (V_{DS}) and gate-to-source (V_{GS}) voltages. Initial sensitivity analysis indicated that the six model elements C_{IN} , R_{IN} , R_{GD} , C_{FB} , R_0 and g_m

exhibited the strongest bias dependence and comprise the dominant device nonlinearities. Subsequently, the other intrinsic model elements together with the package parasitic elements were held fixed in value (linear elements). Comparisons between the fitted model S-parameters and the measured parameters are displayed in Figure 3 for the case of $V_{DS} = 6.0$ VDC and $V_{GS} = -2.0$ VDC. Good agreement is shown not only in the initially modeled 1-10 GHz band but also shown to extend fully into the 10-18 GHz band.

The characterization ultimately led to families of curves drawn to show the bias dependence of each of the six nonlinear model elements. (As an example, the family of curves for C_{IN} is illustrated in Figure 4). Each particular curve relates the calculated (incremental) model element values to the associated drain-to-source voltages. Corrections for the DC voltage drops in the parasitic elements of the device must be made to reference the external or device terminal voltages to internal or intrinsic device voltages. These curves form the basis for this proposed nonlinear model.

Physical Effects and Analytical Predictions

The bias-dependent behavior of each of the nonlinear elements has been studied. The influence of bias on C_{IN} is shown in Figure 4. The initial decreasing values of C_{IN} with increasing V_{DS} and constant V_{GS} is a result of an increasing depletion region width. At values of V_{DS} (indicated by symbols "x" in Figures 1 and 4) where the drain-to-source current (I_{DS}), for $V_{GS} = \text{constant}$, begins to saturate, the active channel capacitance, C_{IN} , approaches a minimum. For further increases in V_{DS} , C_{IN} increases monotonically. This effect was first reported by Engelmann and Liechti.[2] Analytical expressions of Lebovec and Zuleeg, (26) and (14) of [3], were used to calculate the gate-to-source capacitance, $C_{GS}(\text{CALC})$ and transductance, $g_m(\text{CALC})$ parameter values. Calculations were made at the bias conditions required for the onset of drain current saturation. These conditions are designated by the curve $V_{DS,\text{SAT}}$ in Figure 1. The values of $V_{DS,\text{SAT}}$ were determined from laboratory measurements and expression (2) of [3]. Values for the low field mobility, μ , and saturation drift velocity, v_m , used in the analysis were calculated from expressions (10) and (11) of [3]. Values of the saturation current for the Shockley case (I_p) used in (10) and the velocity limited drain current (I_o) used in (11) were determined through extrapolations of the $I_{DS}V_{DS}$ measurements. The calculated $C_{GS}(\text{CALC})$ and $g_m(\text{CALC})$ values with associated bias conditions are listed in Table 1.0. Included in Table 1.0 are corresponding bias values of $C_{GS}(\text{FITTED})$, $g_m(\text{FITTED})$ and $g_m(\text{DC})$. Transconductance, $g_m(\text{DC})$, is derived from the measured $I_{DS}V_{DS}$ device characteristics.

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$C_{GS(FITTED)}$ is equal to the sum of the total excess model capacitance ($C_G + C_{EX}$) and C_{IN} (See Figure 1). The total device excess capacitance is approximately 0.3 pF, a value arrived at from both CV profiling measurements and the device modeled S-parameters. The parameter values $g_m(FITTED)$ are the experimentally derived g_m values. Table 1.0 shows good agreement between the empirically derived and calculated element values.

Predictions of Nonlinear Behavior of GaAs FET's

For simulating nonlinear device-circuit interactions in the time domain, the instantaneous current through each model element must be known as a function of its associated instantaneous voltages as they prevail under arbitrary large-signal drive conditions. The functions describing the instantaneous values of the nonlinear elements are derived from the bias-dependence of the incremental (small-signal) element values discussed above. In each function, the voltage across the input capacitance (C_{IN}) and the voltage across the drain-to-source resistance (R_D) are chosen as independent variables for describing both the instantaneous and the incremental element values. The two expressions for each element are related to one another through a quasi-linear partial differential equation in the two independent variables. Using numerical nonlinear regression techniques the expressions for the instantaneous element values are arrived at in the form of two-dimensional power-series expansions. The use of these expansions may be regarded as a generalization of work reported earlier.^[4] The power series expressions are directly incorporated into a time-domain analysis computer program. The output voltage waveforms for the 600 μ m device in a 50 Ω system were simulated for different drive conditions. This special case was chosen for demonstration to facilitate the acquisition of reliable experimental data for comparison. For each drive condition Fourier analysis was employed to extract frequency-domain information from the waveforms. The comparison between experimental and model-predicted fundamental and harmonic power levels for the device biased at $V_{GS} = -2V$ and $V_{DS} = +6V$ are summarized in Figures 5 and 6. Model-predictions of third-order intermodulation products proved equally reliable.

Conclusions

A technique which accurately predicts nonlinear behavior of GaAs FET's has been presented. The method is based on the experimentally characterized frequency and bias-dependence of device S-parameters. Excellent agreement between experiment and prediction was found for drive levels up to where 6 dB of gain compression occurs.

References

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3. Lebovec, K., Zuleeg, R., "Voltage-Current Characteristics of GaAs J-FETs in the Hot Electron Range," IEEE Solid-State Electronics, Vol.13, pp.1415-1429 (1970)
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TABLE 1.0

BIAS DEPENDENCE OF DEVICE⁽¹⁾ CIRCUIT PARAMETERS AT ONSET OF CURRENT SATURATION

V_{GS}	$V_{DS,SAT}$	(CALC) ⁽²⁾ ($\times 10^{-3}$ MHO's)	(FITTED) ($\times 10^{-3}$ MHO's)	(DC) ⁽³⁾ ($\times 10^{-3}$ MHO's)	$C_{GS}(CALC)(2)(pF)$	$C_{GS}(FITTED)$
0.0	1.9	50	47		0.76	0.76
-1.0	1.7	37	40	41	0.65	0.63
-2.0	1.5	31	32		0.49	0.53
-3.0	1.2	25	22		0.35	0.40
-4.0	0.47	15	9			

⁽¹⁾TEXAS INSTRUMENTS, INC., 600 μ m x 1.7 μ m

⁽²⁾EXPRESSIONS OF LEHOVEC AND ZULEEG [3] AT ONSET OF SATURATION

⁽³⁾DETERMINED FROM $I_{DS}V_{DS}$ CHARACTERISTICS

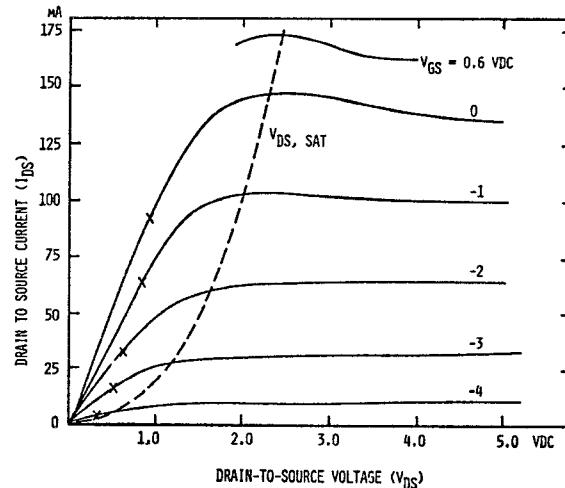


FIGURE 1. MEASURED DC $I_{DS}V_{DS}$ CHARACTERISTICS

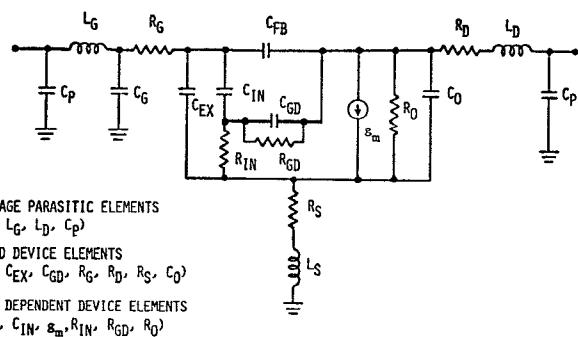


FIGURE 2. CIRCUIT MODEL OF A GAAs MESFET

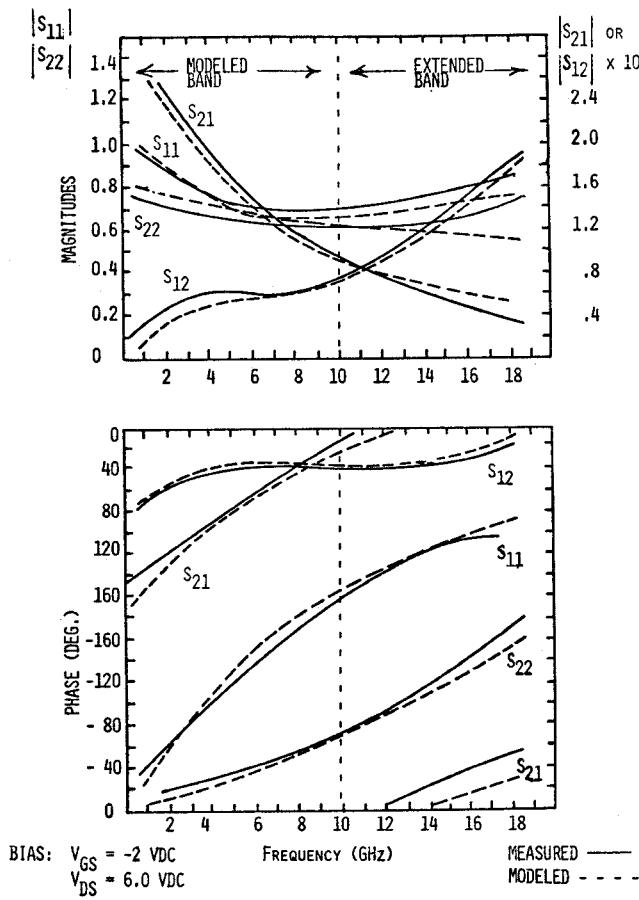


FIGURE 3. S-PARAMETERS (1 TO 18 GHz) FOR GAAS MESFET

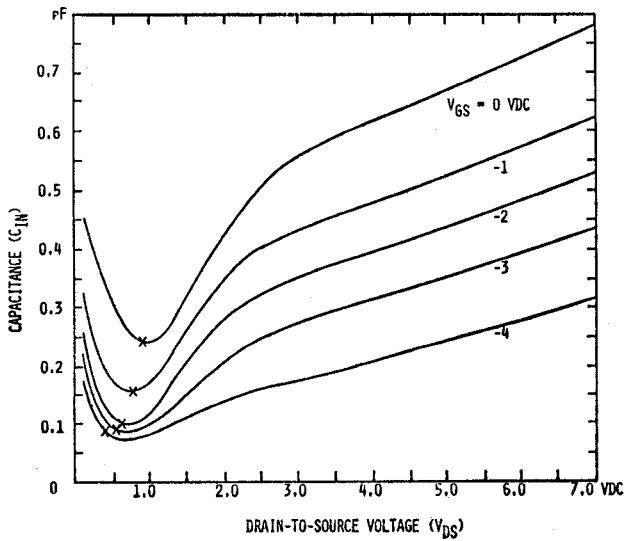


FIGURE 4. BIAS DEPENDENCE OF ACTIVE CHANNEL CAPACITANCE, C_{IN} , FOR A GAAS MESFET

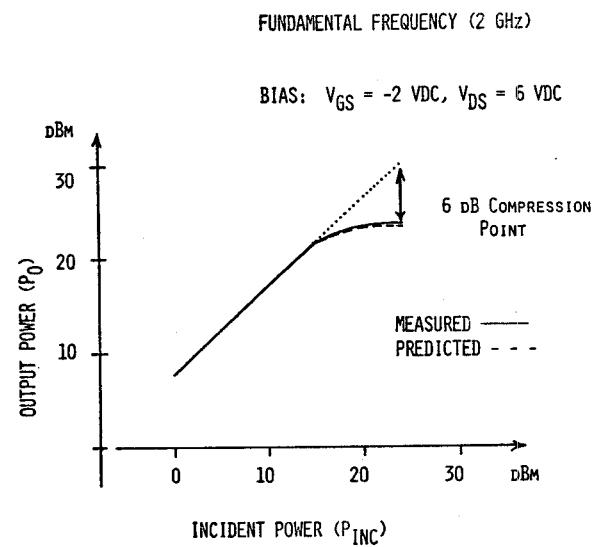


FIGURE 5. FUNDAMENTAL OUTPUT POWER VS. INCIDENT POWER FOR A GAAS MESFET WITH 50 OHM GENERATOR AND OUTPUT LOADS

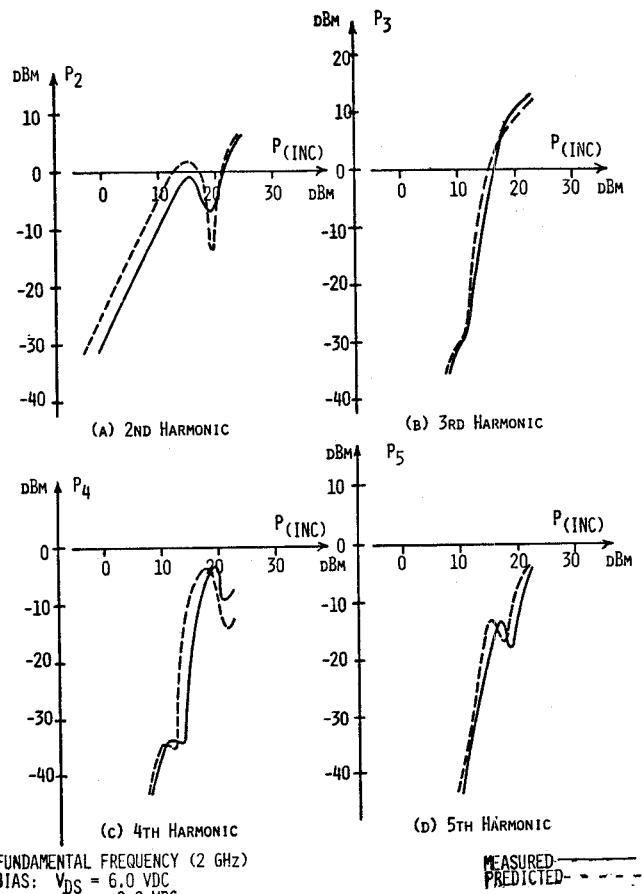


FIGURE 6. HARMONIC OUTPUT POWER LEVELS VS. INCIDENT POWER FOR A GAAS MESFET WITH 50 OHM GENERATOR & OUTPUT LOADS